

VARIABLE STAGE RATIO BUFFER INSERTION FOR NOISE OPTIMIZATION IN A LOGIC NETWORK

FIELD OF THE INVENTION

[0001] The present invention relates to the design of integrated circuits. More specifically, the present invention relates to buffers for use in logic networks.

BACKGROUND OF THE INVENTION

[0002] Optimization of delay in global interconnect paths has long been a goal in the design of integrated circuits. A number of algorithms and design techniques have been used to optimize delay and timing slack in designs utilizing submicron device fabrication technologies. With the continued scaling of process technology, however, unwanted capacitive coupling of signals between adjacent interconnect wires on an integrated circuit becomes a very real problem. This phenomenon is referred to as crosstalk. The occurrence of crosstalk on certain operations can cause a chip to malfunction, for example, when a noise glitch is induced on a metal line as a consequence of a fast switching operation on a nearby line.

[0003] Figure 1 shows an analog model for internally induced crosstalk noise during operation of a logic network. Gate 10 drives net 14 that includes a metal interconnect line with resistance modeled as R_1-R_3 . Capacitors C_1-C_4 represent the capacitive coupling between net 14 and neighboring net 15, which includes gates 11 & 12 and associated physical parameters modeled by resistors R_4-R_8 and capacitors C_5-C_8 . (It is appreciated that inductive coupling may also be present, although not specifically shown in the figure.) In the context of this discussion, net 14 causes the unwanted interference with net 15 by producing an unwanted noise glitch at the input of gate 12 when the output of gate 10 switches

rapidly. In such a model, net 14 is referred to as the aggressor, and net 15, which suffers unwanted interference from the crosstalk-induced glitch, is called the victim. A functional malfunction can occur when the magnitude of the crosstalk-induced glitch is larger than the noise margin at the input node of gate 12 and the resulting glitch propagates to a storage element. When this happens, the logic state of the victim net can flip (e.g., from a logical "1" to a logical "0", or vice-versa).

[0004] One common solution to the problem of network malfunctions caused by glitch noise has been insertion of one or more buffers in the victim net. These buffers are typically selected from a standard cell library and function to distribute the capacitive coupling between the newly created wires. The problem with this approach, however, is that significant additional signal delay can be introduced. Furthermore, often times there is no available space in the existing circuit layout for a set of buffer cells to be added. Moreover, because standard cell buffers are usually optimized for propagation delay, the slew rate tends to be sharper on the newly created wire segments where the buffers have been inserted. This can create new noise problems, i.e., where the victim net becomes the aggressor.

[0005] What is needed, therefore is a new solution to the existing problem of crosstalk in the design of high performance integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention is illustrated by way of example, and not limitation, in the figures of the accompanying drawings, wherein:

[0007] **Figure 1** is a circuit schematic diagram of an analog crosstalk model.

[0008] **Figure 2** is a logic diagram of a size-ratioed buffer in accordance with one embodiment the present invention.

[0009] **Figure 3** is a schematic diagram of a circuit used to compare glitch-suppression of two different buffers.

[0010] **Figure 4** is a graph plotting glitch magnitude versus delay for various size-ratioed buffers in accordance with the present invention.

[0011] **Figure 5** is a graph showing glitch suppression versus time for a buffer in accordance with one embodiment of the present invention.

[0012] **Figure 6** is a schematic diagram illustrating an example of a circuit design in accordance with one embodiment of the present invention.

[0013] **Figure 7** is flow chart of a computer-aided circuit design method according to one embodiment of the present invention.

DETAILED DESCRIPTION

[0014] A variable stage ratio buffer for insertion in a logic network is described. In the following description, specific details are set forth, such as device types, sizes, voltage levels, etc., in order to provide a thorough understanding of the present invention. Practitioners having ordinary skill in the semiconductor arts will understand that the invention may be practiced without many of these details. In other instances, well-known elements, device structures, and processing steps have not been described in detail to avoid obscuring the invention.

[0015] Figure 2 is a logic diagram of a variable stage ratio buffer 20 for use in optimizing noise rejection in an integrated circuit. Buffer 20 comprises a pair of inverters 21 and 22 coupled in series. In one embodiment, each of the inverters are fabricated utilizing conventional complementary metal-oxide semiconductor (CMOS) transistor devices. Other fabrication technologies using different types of devices may also be used.

[0016] Inverter 21 is denoted in Figure 1 as having a device size X, with inverter 22 having a device size Y. According to the present invention, a buffer for optimal noise rejection is created by pairing up different sized inverters wherein the stage ratio X:Y exceeds about 1:6. Depending on the magnitude of the crosstalk-induced noise and the available timing slack, the stage ratio may be 1:22 or larger. In a computer-aided circuit design process, appropriately sized buffers 20 may be inserted at selected locations of the circuit layout to combat crosstalk. This aspect of the present invention will be described in more detail shortly.

[0017] Figure 3 is logic diagram of a test circuit for comparing the response of buffer 20 of the present invention against a conventional buffer 17

taken from a standard cell library. As shown, buffer 17 comprises a pair of series connected inverters 18 & 19 having a standard device size ratio of 1:e ("e" equals approximately 2.6). According to the present invention, buffer 20 is optimized for noise rejection by increasing the device size of the second stage relative to the first. In practice, the first inverter may be sized down and the second inverter sized up to achieve significant glitch suppression. For example, in the circuit of Figure 3, the stage ratio of buffer 20 is 0.5:2e (or approximately 1:10). It is appreciated that stage ratio may be varied by appropriate pairing of different sized inverters to achieve optimal noise, delay, and area requirements for a given net.

[0018] Figure 5 shows a voltage versus time plot of the responses of buffers 17 and 20 to a noise glitch applied simultaneously to each of their inputs. The curve labeled "A" in Figure 5 represents the noise glitch applied to the inputs of buffers 17 & 20. As can be clearly seen, the noise glitch has a magnitude of about 1.2 volts, which is equal to a full rail-to-rail voltage swing of a typical CMOS logic circuit. The slew rate of curve A is approximately 100ps/V.

[0019] The response curve "B" of the response of standard buffer 17 to the noise glitch exhibits virtually no noise rejection to noise glitch A. In fact, the noise is worsened since the noise glitch is widened, increasing the energy of the glitch. The response curve "C" of buffer 20, on the other hand, shows suppression of noise glitch A from 1.2V to 0.15V, with a slight signal delay of about 50ps. Thus, according to the present invention, a buffer with a stage ratio of approximately 1:10 may be utilized to suppress a crosstalk-induced noise glitch on a non-critical signal path, or on a critical path where the available timing slack is greater than about 50ps. Since often times crosstalk glitches tend to occur on non-critical

timing paths, buffer 20 may be inserted into a logic network for noise rejection without impacting the overall speed performance of the design.

[0020] Figure 4 is a plot of noise suppression versus delay for various stage ratios in accordance with the present invention. The curve 30 of Figure 4 shows the noise suppression versus delay tradeoff that can be achieved utilizing the buffer of the present invention. For example, at stage ratios less than about 1:5, virtually no noise rejection is achieved. That is, a crosstalk-induced glitch of magnitude 1.2V is passed to the output with little or no noise suppression. At a stage ratio of about 1:6 and greater significant noise suppression results. By way of example, at a stage ratio of approximately 1:10, noise glitch suppression is sufficient to satisfy typical noise margin levels with minimal signal delay. The plot of Figure 4 also illustrates that for non-critical paths, buffers having a much larger (e.g., 1:22) stage ratio may be utilized. In other words, it is appreciated that the stage ratio of the invented buffer may be varied to optimize glitch noise suppression depending on the timing slack available at a particular node in the network.

[0021] In another aspect of the present invention, insertion of a variable stage ratio buffer into a logic network occurs during a computer-aided design process after layout of device cells and interconnects. This point in the process is represented in the flow chart of Figure 7 by block 41. Following placement of all cells and wires, well-known software tools may be used to extract circuit parameters such as capacitance, inductance, resistance, etc. This parametric information can then be used in conjunction with standard analysis tools to identify signal paths prone to crosstalk-induced noise glitches. Extraction and analysis tools may also be used to identify critical timing paths and timing slack available

at various nodes within the network. Typically, such analysis is performed assuming worst-case noise conditions, as indicated in block 42.

[0022] In one embodiment of the method of the present invention, noise is allowed to propagate until it arrives at the input of a state-preserving device such as a flip-flop, latch, register, or the like. The noise glitch is then analyzed to determine whether it is of a magnitude sufficient to possibly cause a malfunction or functional failure of the circuit (block 43). The available slack in the timing path may also be determined at this point. A noise suppression buffer is then inserted at the input of the state device, as shown by block 44. In one implementation, the buffer is selected with a stage ratio that provides adequate noise suppression without violating any critical timing in the signal path.

[0023] Figure 6 is a circuit diagram illustrating the end result of the above-described method of the present invention. A crosstalk-induced noise glitch is first determined to exist on net 34, propagating to the input of D-type flip-flop device 40. The magnitude of the glitch and the available timing slack at the input node of device 40 is utilized to select a buffer 20 having an appropriate stage ratio to provide sufficient noise suppression with a delay within the available timing margin. In this example, the logic network is modified by the insertion of buffer 20 as close as possible to the input of device 40. Finally, the circuit may optionally be re-analyzed to confirm noise and timing margins have not been violated.